REMARKS

Summary of Office Action

Claims 1-21 are pending. Claims 10-21 were withdrawn from consideration as drawn to a non-elected invention.

Claims 1-9 have been rejected under 35 U.S.C. 102(b) as being anticipated by Sato U.S. Patent No. 6,124,725 ("Sato"). The Examiner also has objected to informalities in claim 1.

Applicants' Reply

Applicants have amended claim 1 to correct the informality that was kindly noted by the Examiner, and further to clarify the invention. Applicants respectfully traverse the prior art rejections of claims 1-9.

Applicants' invention relates to testing of motion-sensitive substrate elements (e.g., Micro-Electro-Mechanical Systems (MEMS) devices such as accelerometers used in automobile airbags). The elements of method claim 1 include (1) contacting the substrate with contact needles to measure electrical properties of substrate elements, and (2) during such measurement accelerating the substrate which brings out motion sensitive characteristics.

Applicants respectfully submit that Sato does not teach, show or suggest accelerating a substrate during measurement. Sato describes a testing apparatus designed to alternately conduct reliability testing and electrical testing of semiconductor wafers. Sato's apparatus includes a switch mechanism for switching between reliability test mechanisms and electrical test mechanisms. (See e.g., Abstract, col. 2 lines 21-43, etc.). Further, Sato describes a conventional motorized X-Y-Z and Θ table (i.e. a linear motion and rotation stage) for mechanically indexing or advancing the substrate so that different chips on the substrate can be

sequentially positioned under probes for testing. (See e.g., col. 4, lines 6-23). The portions of Sato cited by the Examiner (i.e. col. 4 lines 50-55) describe high and low "speed" electrical AC testing to determine if the substrate chips are "good or bad." Applicants respectfully submit that Sato's "speed" refers to the rate at which electrical measurements on "stationary" chips are conducted or the rate at which substrate chips are indexed in X or Y directions through the testing apparatus prior to testing or measurements.

Applicants note that Sato at col. 7 line 38 to col. 9 line 24 describes a procedure for proper alignment or orientation of the substrate relative to the test apparatus prior to testing or measurements. Portions of Sato cited by the Examiner (i.e., col. 8 lines 65-68) refer to rotational alignment of the substrate wafer so that the X-Y co-ordinates of the chip pattern are properly aligned with the X-Y axes of the motorized stage for linear indexing from one chip to another. (See col. 8 lines 53- col. 9 line 4).

All of Sato's testing or measurement take place when the substrate is stationary or at "halt" after the appropriate chips under test are properly aligned with the contractor (prober). (See e.g., col. 9 lines 21-24). Sato, in particular, does not show teach or suggest "accelerating the mounted semiconductor substrate in contact with the contact needles while measuring the electrical characteristics of the circuit elements" as is required by applicants' claim 1.

For at least the foregoing reasons, claim 1 and also dependent claims 2-9 are patentable over Sato.

Conclusion

Applicants respectfully submit that this application is now in condition for allowance. Reconsideration and prompt allowance of which are respectfully requested. If there are any remaining issues to be resolved, applicants respectfully request that the Examiner kindly contact the undersigned attorney for early resolution.

Respectfully submitted,

By: _____

Manu J. Tejwani
Patent Office Reg. No. 37,952

Baker Botts L.L.P
30 Rockefeller Plaza
44th Floor
New York, NY 10012-4498

Attorneys for Applicants
212-408-2614